AMENDMENTS TO THE CLAIMS

Claims 1-13 (canceled)

14. (previously presented) A memory circuit, comprising:

an array of single bit nonvolatile memory cells organized in columns, wherein each of the memory cells comprises a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein:

adjacent memory cells in each column of the memory circuit have one of their sources and their drains in common;

the sources of the memory cells in each column of the memory circuit are coupled with the same bitline, the bitline running parallel with the column;

the drains of the memory cells in each column of the memory circuit are coupled with a respective program line, the program line running perpendicular to the column; and

the gates of the memory cells in each column of the memory circuit are coupled with a respective word line, the word line running perpendicular to the column,

wherein programming a memory cell of the memory circuit comprises:

applying electrical ground to a first bitline;

applying a first voltage having a first polarity to a wordline;

applying a second voltage of the first polarity to a program line;

applying a third voltage, having a second polarity opposite to the first polarity to the semiconductor substrate; and

applying a fourth voltage of the first polarity to all other bitlines of the memory circuit.

McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, Illinois 60606
Phone (312) 913-0001
Facsimile (312) 913-0002

Claim 15 (canceled)

Claim 16 (previously presented) The memory circuit of claim 14, wherein absolute values of each of the first, second and third voltages are 5 V or less, and an absolute value of the fourth voltage is 2 V or less.

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Facsimile (312) 913-0002